REMARKS

Claims 1-11 are pending. Claims 1-11 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

In the Abstract and Specification

The abstract and the specification were objected to as containing minor informalities. Applicant has amended the abstract and the specification to correct these informalities. Accordingly, Applicant respectfully submits that this objection is moot.

Claim Objections

The claims 1 and 7 were objected to as containing grammatical errors. Applicant has amended claims 1 and 7 to correct these grammatical errors. Accordingly, Applicant respectfully submits that this objection is moot.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-11 were rejected under 35 U.S.C. § 103(a) over Williams (U.S. Patent No. 6,745,338) in view of Hui et al. (U.S. Patent No. 6,694,463). Applicant respectfully traverses this rejection.

Claim 1 recites, in part, a microcontroller that includes a first switch for transmitting an internal signal of the microcontroller to a clock output pin for using the clock output pin in a predetermined system mode and a second switch, which is coupled between the clock generating means and the clock output pin and enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode. As admitted in the Office Action on page 3, Williams fails to disclose, teach , or suggest such a feature. The Office Action alleges that Hui teaches the above features of claim 1. Applicant respectfully disagrees.

Hui merely discloses test mode buffers 44 and 46 and normal buffers 24 and 34. The test mode buffers 44 and 46 are connected in series to one another and an output of the buffer 44 is input into the buffer 46, and the buffer 46 has an output 63 (Figure 2). Therefore, the outputs of buffers 44 and 46 are different whereas the first and second switches in claim 1 are the same (namely, the clock output pin). Accordingly, no combination of Williams and Hui teach or suggest a microcontroller that includes a first switch for transmitting an internal signal of the microcontroller to a clock output pin for using

the clock output pin in a predetermined system mode and a second switch, which is coupled between the clock generating means and the clock output pin and enabled in the clock generation mode for transmitting the clock signal between the clock generating means and the clock output pin and disabled in the predetermined system mode, as recited in claim 1.

Claim 7 is believed allowable for at least the reasons presented above with respect to claim 1 because claim 7 recites the same feature of claim 1 discussed above.

Claims 2-6 and 8-11 are believed allowable for at least the same reasons presented above with respect to claims 1 and 7 by virtue of their dependence upon claims 1 and 7. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

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